CLAIMS

What is claimed is:

1. An integrated circuit device comprising:

a receive circuit to capture a plurality of samples of an input signal during a cycle of a first clock signal;

a select circuit coupled to the receive circuit to select, according to a data rate select signal, one of the plurality of samples to be a first selected sample of the input signal and another of the plurality of samples to be a second selected sample of the input signal; and

a phase control circuit coupled to receive the first and second selected samples of the input signal and being adapted to compare the first selected sample with the second selected sample to determine whether the first clock signal leads or lags a transition of the input signal.

2. The integrated circuit device of claim 1 wherein the select circuit selects a first pair of the plurality of samples of the input signal to be the first and second selected samples if the data rate select signal is in a first state, and the select circuit selects a second pair of the plurality of samples of the input signal to be the first and second selected samples if the data rate select signal is in a second state, the second pair of the samples including at least one sample of the input signal that is not included in the first pair of the samples.

3. The integrated circuit device of claim 2 wherein the phase control circuit generates an early/late indicator to indicate that the first clock signal leads the transition of the input signal if the first selected sample has the same state as the second selected sample.

4. The integrated circuit device of claim 2 wherein the select circuit further selects a third sample of the plurality of samples to be a third selected sample, the first and the third selected samples being successive samples of a data state of the input signal and the second selected sample being a data transition sample of the input signal.

5. The integrated circuit device of claim 4 wherein the phase control circuit includes an early/late detection circuit to compare the first and third selected samples to determine whether a transition has occurred in the input signal.

6. The integrated circuit device of claim 5 wherein the early/late detection circuit includes circuitry to generate an output signal to indicate that the first clock signal leads the transition of the input signal if the first and third selected samples indicate that a transition has occurred in the input signal and if the second selected sample is determined to have the same state as the first selected sample.

7. The integrated circuit device of claim 1 wherein the first clock signal comprises a plurality of component clock signals each being offset in phase from one another.

8. The integrated circuit device of claim 1 wherein the first clock signal comprises M component clock signals each having a respective phase angle such that transitions of the component clock signals occur at evenly spaced intervals within a cycle of a first one of the component clock signals.

9. The integrated circuit device of claim 8 wherein the receive circuit comprises M sampling circuits each being responsive to a respective one of the component clock signals to sample

the input signal such that M samples of the input signal are captured during each cycle of the first clock signal.

10. The integrated circuit device of claim 9 wherein the receive circuit further comprises M shift registers, each shift register being coupled to a respective one of the M sampling circuits to receive samples of the input signal therefrom, each shift register including N storage locations to store a new set of N samples of the input signal every N cycles of the first clock signal.

11. The integrated circuit device of claim 1 further comprising a storage circuit to store a data rate select value indicative of a data rate of the input signal, the data rate select signal having a state according to the data rate select value.

12. The integrated circuit device of claim 11 wherein the storage circuit includes an output to output the data rate select signal to the select circuit.

13. The integrated circuit device of claim 11 further comprising circuitry to receive the data rate select value from an external device and to store the data rate select value in the storage circuit.

14. A clock data recovery (CDR) circuit comprising:

a plurality of sampling circuits to capture a plurality of samples of an input signal during a cycle of a first clock signal;

a sample steering circuit coupled to receive the plurality of samples from the sampling circuits and being adapted to select data state samples and data transition samples from among the plurality of samples according to a data rate select signal; and

a phase control circuit coupled to receive the selected data state samples and data transition samples and including circuitry to compare the selected data state and data transition samples to determine whether the first clock signal leads or lags transitions in the input signal.

15. The CDR circuit of claim 14 wherein the phase control circuit includes circuitry to generate a phase control signal having a state according to whether the first clock signal leads or lags transitions in the input signal.

16. The CDR circuit of claim 15 further comprising a phase mixer circuit to interpolate between a selected pair of phase vectors to generate the first clock signal, the phase mixer being coupled to receive the phase control signal from the phase control circuit and being adapted to adjust the phase of the recovered clock signal according to the state of the phase control signal.

17. The CDR circuit of claim 14 wherein the selected data state samples and data transition samples are obtained from a first set of sampling circuits within the plurality of sampling circuits when the data rate select signal is in a first state, and from a second set of sampling circuits within the plurality of sampling circuits when the data rate select signal is in a second state, the second set of sampling circuits including at least one sampling circuit that is not included in the first set of sampling circuits.

18. A method of operation within an integrated circuit device, the method comprising:

capturing a plurality of samples of an input signal during a cycle of a first clock signal;

selecting a first data state sample and a first data transition sample from among the

plurality of samples according to a data rate select signal; and

comparing the first data state sample and the first data transition sample to determine whether the first clock signal leads or lags a transition of the input signal.

19. The method of claim 18 wherein selecting the first data state sample and the first data transition sample comprises selecting a first pair of the plurality of samples to be the first data state sample and the first data transition sample if the data rate select signal is in a first state, and selecting a second pair of the plurality of samples to be the first data state sample and the first data transition sample if the data rate select signal is in a second state, the second pair of the plurality of samples including at least one sample that is not included in the first pair of the plurality of samples.

20. The method of claim 18 further comprising adjusting a phase of the first clock signal based in part on the comparison of the first data state sample and the first data transition sample.

21. The method of claim 18 wherein comparing the first data state sample and the first data transition sample to determine whether the first clock signal leads or lags the transition in the input signal comprises determining whether the first data state sample has the same value as the data transition sample.

22. The method of claim 18 wherein comparing the first data state sample and the first data transition sample to determine whether the first clock signal leads or lags the transition in the input signal comprises comparing the first data state sample to a second data state sample to determine whether a transition occurred in the input signal in the interval between the first data state sample and the second data state sample.

23. The method of claim 18 wherein capturing a plurality of samples of the input signal during a cycle of a first clock signal comprises sampling the input signal in response to a plurality of sampling clock signals that each transition at least once per cycle of the first clock signal and that are each phase offset from one another.

24. The method of claim 23 wherein the first clock signal is one of the sampling clock signals.

25. The method of claim 18 further comprising generating the data rate select value according to a data rate select value stored in a configuration storage circuit within the integrated circuit device.

26. The method of claim 25 further comprising receiving the data rate select value via an external interface of the integrated circuit device and storing the data rate select value in the configuration storage circuit.

27. A method of controlling an integrated circuit device, the method comprising:

outputting a data rate select value to the integrated circuit device; and

outputting a command to the integrated circuit device to store the data rate select value in a configuration storage circuit within the integrated circuit device, the configuration storage circuit being coupled to a clock data recovery (CDR) circuit within the integrated circuit device to control the selection of samples of an input signal used for recovering a clock signal from the input signal.

28. The method of claim 27 wherein outputting the data rate select value comprises outputting a configuration instruction to the integrated circuit device, the data rate select value

constituting operand data of the configuration instruction.

29. The method of claim 27 wherein outputting the data rate select value comprises outputting a configuration instruction to the integrated circuit device, the data rate select value constituting an operation code of the configuration instruction.

30. The method of claim 27 wherein outputting a data rate select value to the integrated circuit device comprises outputting a value indicative of a number of data values included within the input signal per cycle of the clock signal.

31. An integrated circuit device comprising:

an output driver to output a signal onto a data path;

a serializing circuit to receive a first parallel set of bits and coupled to output the set of bits in sequence to the output driver in response to a first clock signal; and

a select circuit coupled to the serializing circuit and having an input to receive an outbound data value, the select circuit being adapted to select, according to a data rate select signal, data bits within the outbound data value to form the first parallel set of bits received within the serializing circuit.

32. The integrated circuit device of claim 31 wherein, when the data rate select signal indicates a first data rate, the select circuit is adapted to select a first portion of the outbound data value to form the first parallel set of bits and to select a second portion of the outbound data value to form a second parallel set of bits to be received within the serializing circuit after the first parallel set of bits.

33. The integrated circuit device of claim 32 wherein each bit of the first portion of the

outbound data value is used to source at least a pair of bits in the first parallel set of bits.

34. The integrated circuit device of claim 32 wherein, when the data rate select signal indicates a second data rate, the select circuit is adapted to select the entire outbound data value to form received the first parallel set of bits.

35. The integrated circuit device of claim 33 wherein the first data rate is a single data rate and the second data rate is a double data rate.

36. A method of operation within an integrated circuit device, the method comprising:

outputting a first parallel set of bits in sequence in response to a transmit clock signal to form an output signal; and

selecting the first parallel set of bits from among a plurality of data bits within an outbound data value in a sequence according to a data rate select signal to achieve a selected data rate within the output signal.

37. The method of claim 36 wherein selecting the first parallel set of bits from among the plurality of data bits within an outbound data value in a sequence according to a data rate select signal comprises selecting all the data bits within the outbound data value to form the first parallel set of bits when the data rate select signal is in a first state, and selecting a portion of the data bits within the outbound data value to form the first parallel set of bits when the data rate select signal is in a second state.

38. The method of claim 37 wherein selecting the portion of the data bits within the outbound data value to form the first parallel set of bits comprises sourcing each pair of bits within the first parallel set of bits with a respective bit of the portion of the data bits within the

outbound data value.

39. A method of controlling an integrated circuit device, the method comprising:

outputting a data rate select value to the integrated circuit device; and

outputting a command to the integrated circuit device to store the data rate select value in a configuration storage circuit within the integrated circuit device, the configuration storage circuit being coupled to a transmit circuit within the integrated circuit device to select either a first output order or a second output order of data bits within respective outbound data values, the first output order corresponding to a first output data rate and the second output order corresponding to a second output data rate.

40. The method of claim 39 wherein outputting the data rate select value comprises outputting a configuration instruction to the integrated circuit device, the data rate select value constituting operand data of the configuration instruction.

41. The method of claim 39 wherein outputting the data rate select value comprises outputting a configuration instruction to the integrated circuit device, the data rate select value constituting an operation code of the configuration instruction.